AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit in which a device for high-speed access, ~~a~~ two or more devices for lower-speed access and a control circuit for controlling transfers of data ~~to~~ with these devices are connected by a common bus in such a manner that transfers of data ~~to~~ with the device for high-speed access takes priority over data transfers with the devices for lower-speed access, said integrated circuit comprising:

a plurality of switch circuits, each for performing control to turn on and off the bus connection between the device for high-speed access and a corresponding one of the devices for lower-speed access; and

at least one switch control circuit for controlling said switch circuits so as to turn off the bus connection between the device for high-speed access and each of the devices for lower-speed access when data is transferred to the device for high-speed access, and turn on the bus connection between the device for high-speed access and at least one of the devices for lower-

speed access when data is transferred to at least one of the devices for lower-speed access,

wherein the device for high-speed access, the devices for lower-speed access and the switch control circuit each operates in synchronization with common clock pulses, the common clock pulses having a period that varies based on the access speed of the device to be accessed.

2. (Currently Amended) The integrated circuit according to claim 1, wherein ~~a plurality of devices inclusive of~~ the device for high-speed access and the devices for lower-speed access are connected by the common bus so as to be given priority for data transfer in order of decreasing access speed;

each of said switch circuits being provided between mutually adjacent devices among said ~~plurality of~~ devices for high-speed access and lower-speed access in order to turn~~ing~~ on and off the bus connection between the mutually adjacent devices among said plurality of devices;

said switch control circuit controlling said switch circuits in sequence so as to turn on the respective bus connections so as to ~~make possible~~ enable access to ~~a device circuit having a~~ devices of higher access speed before enabling access to devices of lower access speed.

3. (Currently Amended) The integrated circuit according to claim 1, wherein said ~~integrated circuit further comprises a~~ control circuit ~~for outputting~~ is configured to output, in sync with the common clock pulses, a data-transfer enable signal that enables transfer of data upon elapse of a fixed period of time after said switch control circuit controls each of said switch circuits so as to turn on the bus connection.

4. (Currently Amended) The integrated circuit according to claim 3, wherein output timing of the data-transfer enable signal output from said ~~output~~ control circuit differs in dependence upon the access speeds of said devices.

5. (Canceled)

6. (Currently Amended) A method of controlling an integrated circuit in which a device for high-speed access, ~~a~~ two or more devices for lower-speed access and a control circuit for controlling transfer of data ~~to~~ with these devices are connected by a common bus in such a manner that transfers of data ~~to~~ with the device for high-speed access takes priority over data

transfers with the devices for lower-speed access, said method comprising:

providing a plurality of switch circuits, each for performing control to turn on and off the bus connection between the device for high-speed access and a corresponding one of the devices for lower-speed access;

controlling the switch circuits so as to turn off the bus connection between the device for high-speed access and each of the devices for lower-speed access when data is transferred to the device for high-speed access and turn on the bus connection between the device for high-speed access and at least one of the devices for lower-speed access when data is transferred to at least one of the devices for lower-speed access; and

operating the device for high-speed access, the devices for lower-speed access and the switch control circuit in synchronization with common clock pulses, the common clock pulses having a period that varies based on the access speed of the device to be accessed.

7. (New) The method according to claim 6, further comprising:

connecting the device for high-speed access and the devices for lower-speed access by the common bus so as give priority for

data transfer to the connected devices in order of decreasing access speed;

providing each of said switch circuits between mutually adjacent devices among said devices for high-speed access and lower-speed access in order to turn on and off the bus connection between the mutually adjacent devices among said plurality of devices; and

controlling said switch circuits in sequence so as to turn on the respective bus connections so as to enable access to devices of higher access speed before enabling access to devices of lower access speed.

8. (New) The integrated circuit according to claim 6, further comprising:

outputting, in sync with the common clock pulses, a data-transfer enable signal that enables transfer of data upon a fixed period of time elapsing after controlling each of the switch circuits to turn on the bus connection.

9. (New) The integrated circuit according to claim 8, wherein output timing of the data-transfer enable signal output from said control circuit differs in dependence upon the access speeds of said devices.

10. (New) An integrated circuit comprising:

three or more devices configured to operate in synchronization with a common clock signal, the devices including a first device configured for high-speed access and at least two devices configured for lower-speed access relative to the first;

a processor configured to control data transfers for each of the devices; and

a bus operably connecting each of the devices to the processor such that the data transfers are performed over the bus, the bus including a switch for each of the lower-speed access devices,

wherein each switch is configured to disable a bus connection between the corresponding lower-speed access devices and the processor when a data transfer is performed with the high-speed access device, and

wherein a period of the common clock signal varies based on an access speed of the device associated with the data transfer being performed over the bus.

11. (New) The integrated circuit according to claim 10, further comprising:

at least one switch controller configured to control each of the switches to disable the bus connection to the corresponding lower-access speed device when a data transfer is being performed with the first device, and to enable the bus connection to the corresponding lower-access speed device when a data transfer is being performed with the corresponding lower-access speed device.

12. (New) The integrated circuit according to claim 10, wherein each switch comprises a metal oxide semiconductor (MOS) connected to the bus.

13. (New) The integrated circuit according to claim 10, the lower-speed access devices including second and third devices, wherein:

a first portion of the bus operably connects the first device to the processor, a second portion of the bus operably connects the second device to the first portion of the bus, and a third portion of the bus connects the third device to the second portion of the bus, and

the switch for the second device is configured to selectively enable and disable the second portion of the bus,

and the switch for the third device is configured to selectively enable and disable the third portion of the bus.

14. (New) The integrated circuit according to claim 13, wherein the second device is configured for higher-speed access than the third device.

15. (New) The integrated circuit according to claim 14, further comprising at least one switch controller configured to:

control the switch for the second device to disable the second portion of the bus when a data transfer is being performed with the first device, and to enable the second portion of the bus when a data transfer is being performed with the second device; and

control the switch for the third device to disable the third portion of the bus when a data transfer is being performed with the second device, and to enable the third portion of the bus when a data transfer is being performed with the third device.

16. (New) The integrated circuit according to claim 15, wherein the at least one switch controller comprises a plurality of switch controllers, one of the switch controllers being

configured to control the switch for the second device, and another one of the switch controllers being configured to control the switch for the third device.

17. (New) The integrated circuit according to claim 15, wherein the switch for the second device comprises a metal oxide semiconductor (MOS) connected to the second portion of the bus, and the switch for the third device comprises a MOS connected to the third portion of the bus.

18. (New) The integrated circuit according to claim 10, wherein the devices are connected at respective points of the bus, such that the relative distances between the processor and the connection points of the devices increase as the operating speed of the respective devices decrease.